

FIG. 1

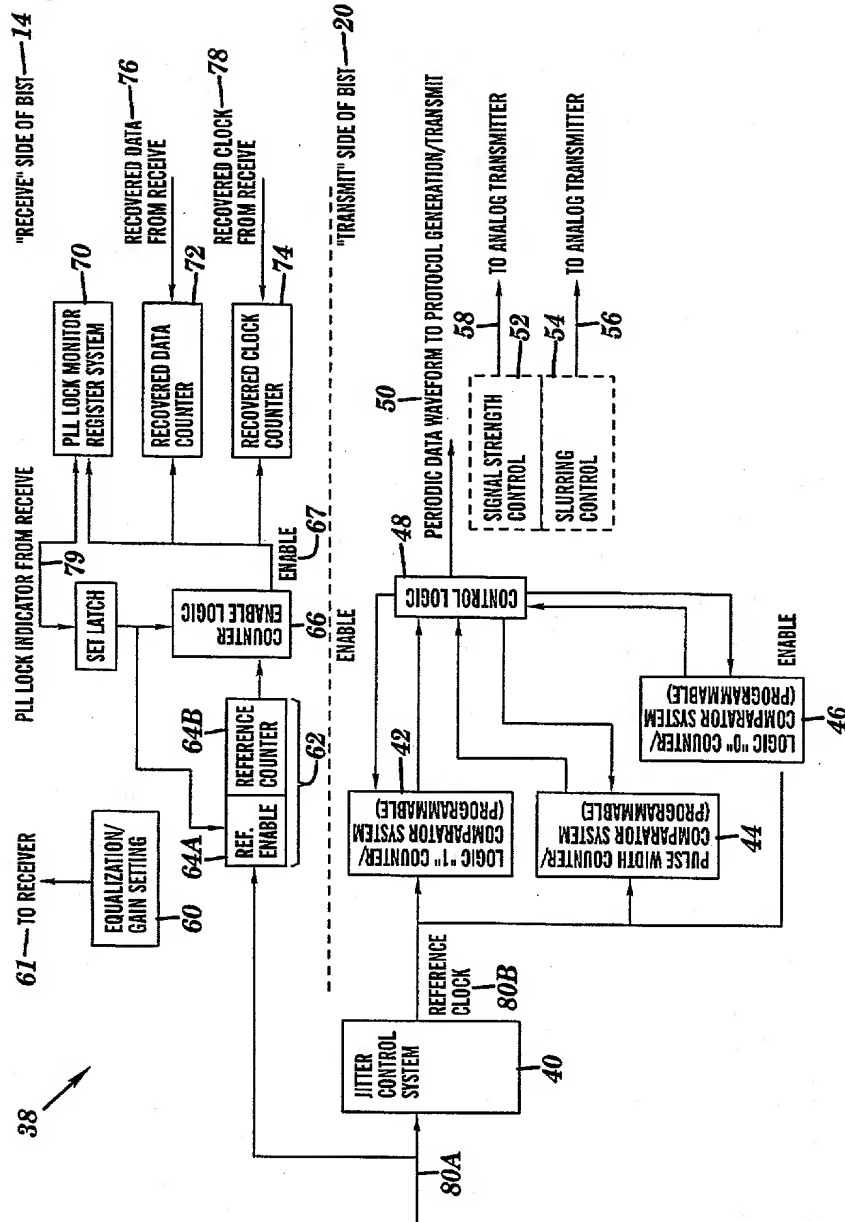


FIG. 2

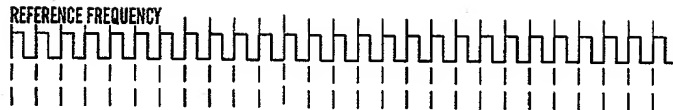


FIG. 3A

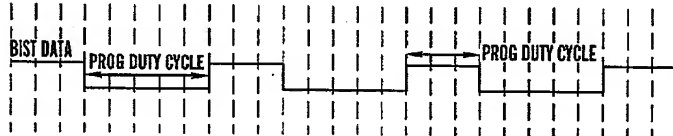


FIG. 3B

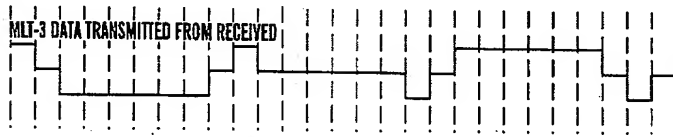


FIG. 3C

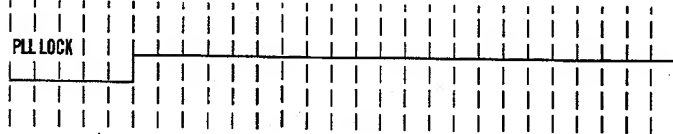


FIG. 3D

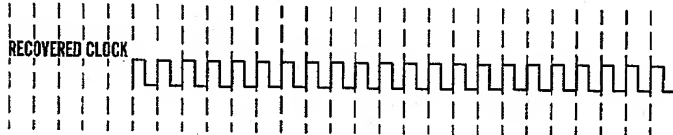


FIG. 3E

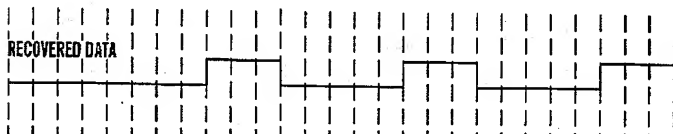


FIG. 3F

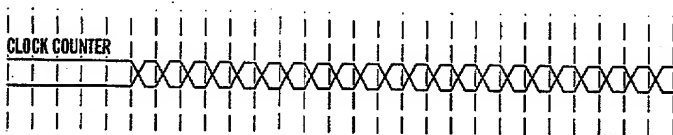


FIG. 3G

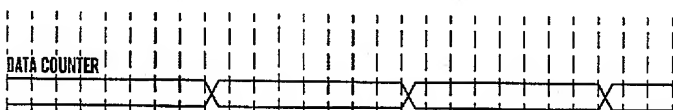


FIG. 3H

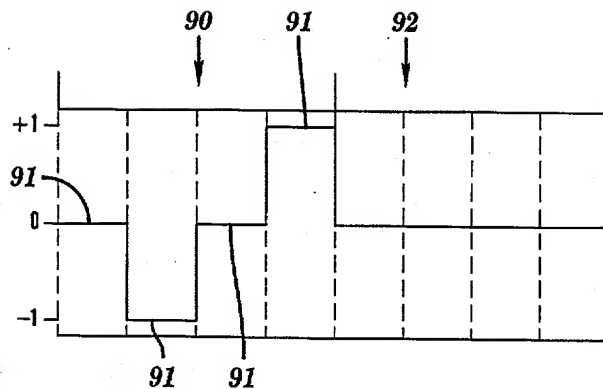


FIG. 4A

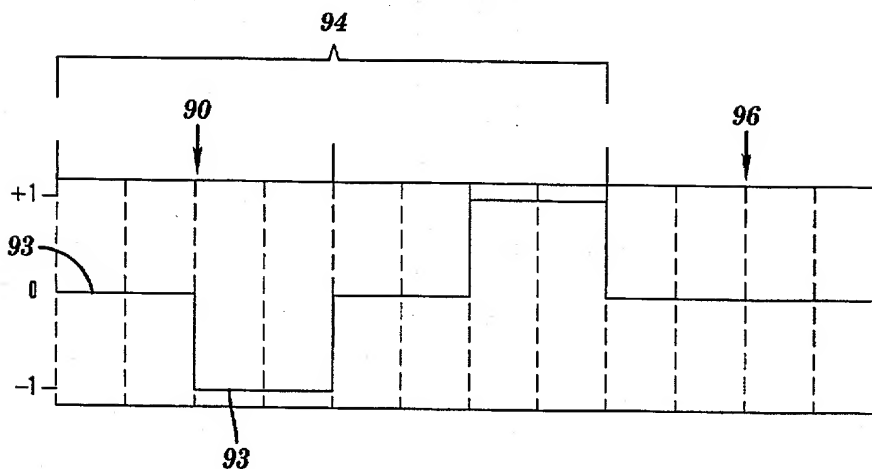


FIG. 4B

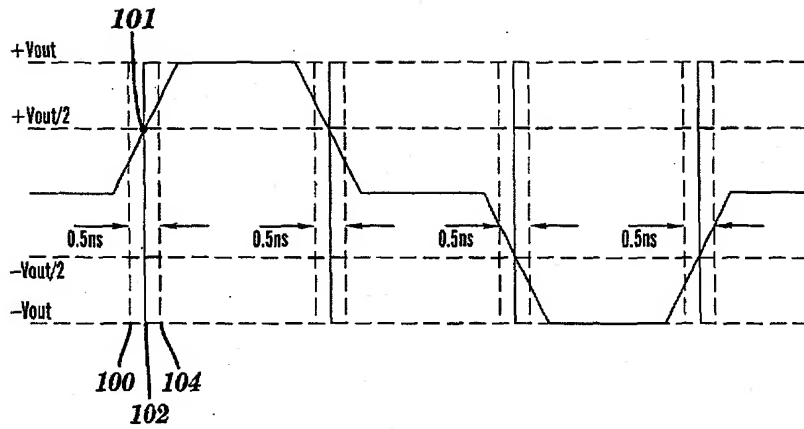


FIG. 5




FIG. 7A Cin  80A


FIG. 7B Cearly  120

FIG. 7C Cnom  122


FIG. 7D Clate  124

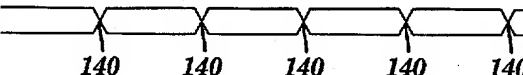
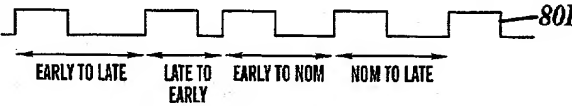
FIG. 7E MUX CONTROL  140 140 140 140 140

FIG. 7F SYSTEM CLOCK (EDGE TRIGGERED)  80B
EARLY TO LATE LATE TO EARLY EARLY TO NOM NOM TO LATE

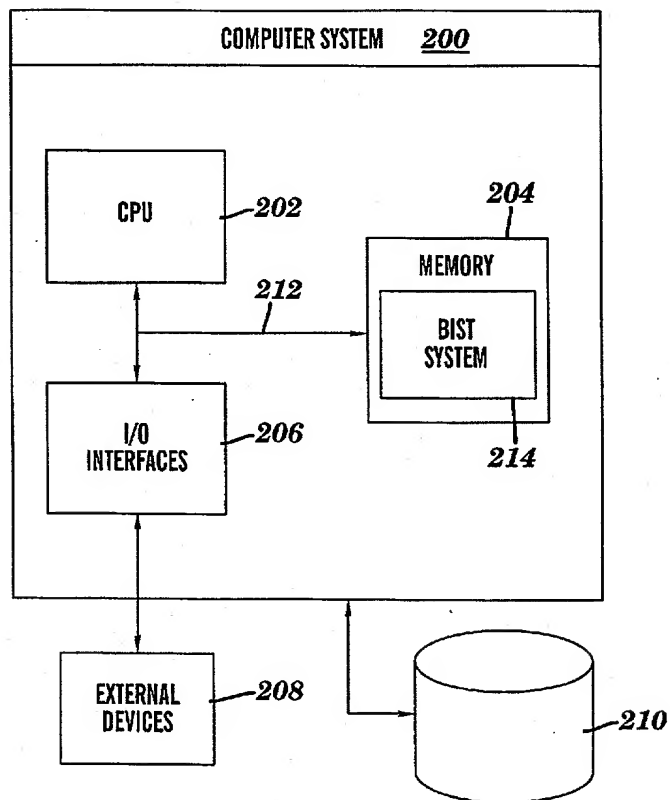


FIG. 8